

CAISO Dynamic Model Validation Procedure for Inverter-Based Resources

This document describes the positive sequence dynamic model validation procedure for inverter-based resources (IBR) that are required for interconnection requests and operational resources.

1 Dynamic model validation in GE PSLF

1.1 Stand-alone model validation

The power flow and dynamic models are tested by adding a voltage source at the POI. The CAISO developed a tool to test model performance at different system strength levels. The structure of the tool is shown below.

Table 1: File Structure

Folder	Description	Files
.	Working folder where PSLF is invoked	<ul style="list-style-type: none">• IBR_model_test.p (main program)• prerun_setGThevn.p (set SCR to n)• CheckREModels.p (extract control settings)• Runs_IBR_Tests.runs (define test runs)
.\cases\	Power flow cases	*.sav
.\dyds\	Dynamic models and contingencies	<ul style="list-style-type: none">• *.dyd (dynamic model)• Flat.p (flat run)• Bump.p (fault at POI)• Vstep_(a/b).p (plant controller voltage reference step change)• Fstep_(a/b).p (plant controller frequency reference step change)• Qstep_b.p (plant controller Q reference step change)• Play_vrt.csv (play-back voltage signal for voltage ride-through test)
.\chans\	Simulation output files	<ul style="list-style-type: none">*.log (simulation log file)*_event.csv (event file)*.chf (channel file)

1.1.1 Data preparation

Power flow data

Power flow model (.epc) – set the POI bus to type 0; add an infinite generator to the POI bus (Thevenin equivalent gen).

Load the epc and solve at the desired MW output. Depending on the type of the plant, multiple dispatch conditions may be created and tested. The table below shows the recommended dispatch scenarios.

Table 2: Dispatch Scenarios

Plant Type	Dispatch Scenarios	Notes
Wind and/or Solar	Pgen slightly lower than Pmax	Leave some headroom (e.g. 10%) for frequency response test
Stand-alone BESS	Pgen slightly lower than Pmax	Leave some headroom (e.g. 10%) for frequency response test
	Pgen slightly higher than Pmin	Leave some headroom (e.g. 10%) for frequency response test
	Online with Pgen=0	Test BESS voltage control and frequency control at no active power output
Hybrid BESS and other types of generators	BESS discharging and other generators off	Test BESS control performance; leave some headroom on BESS (e.g. 10%) for frequency response test
	BESS charging and other generators off <i>if the plant charges from the grid</i>	
	BESS off and other generators on	Test other generators control performance; leave some headroom on the other generators (e.g. 10%) for frequency response test
	BESS discharging and other generators on with net MW < plant MW	Test control coordination between BESS and other generators
	BESS charging and other generators on with net MW = 0	

Save the power flow in .\cases\xxxx.sav

Dynamic data

Copy the dynamic model to .\dyds\xxxx.dyd. Perform a visual review of the models, e.g. proper models are used, models are entered in the right format, models are invoked properly, etc. Make sure it does not include gen model for the generator added at the POI bus. Edit the following files to use the POI bus number.

Thevenin.dyd: Dynamic model for the Thevenin gen

TheveninPB.dyd: Playback model for the Thevenin gen

Bump.p: 3-phase fault at POI

Edit the following files to use the repc_* invoking bus number.

Vstep_*.p or qstep_b.p: voltage/reactive power reference change in repc_* model

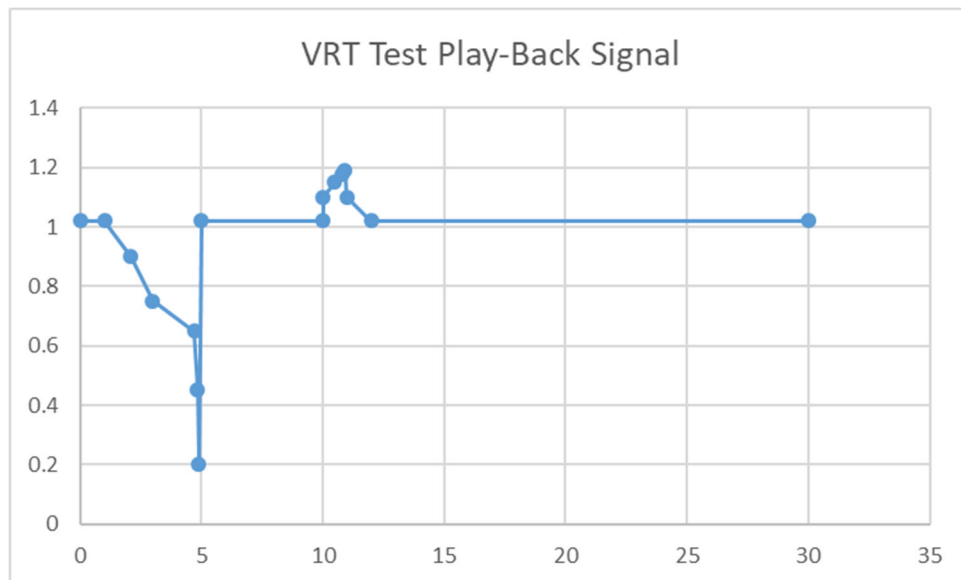
Fstep_*.p: frequency reference change in repc_* model

Play-back Signal

A voltage profile is defined in play_vrt.csv:

Table 3: Voltage Profile for Ride-Through Test

t	v	
0	1.02	Modify to match initial voltage in the base case
1	1.02	Modify to match initial voltage in the base case
2.1	0.9	
3	0.75	
4.7	0.65	
4.85	0.45	
4.9	0.2	
5	1.02	
10	1.02	
10.02	1.1	
10.5	1.15	
10.8	1.175	
10.9	1.19	
11	1.1	
12	1.02	
30	1.02	



The table below shows the cumulative duration of voltage below or above the PRC-024:

Table 4: Cumulative Duration of the Voltage Profile

Voltage (p.u.)	Duration (sec)
≤ 0.45	0.15
≤ 0.65	0.3
≤ 0.75	<2
≤ 0.9	<3
≥ 1.10	<1
≥ 1.15	<0.5
≥ 1.175	<0.2

With this profile, the generator should remain connected and produce active and reactive outputs.

Set up the runs

Set up the runs in Runs_IBR_Tests.runs. Each run is defined by

- Power flow case
- pre-run epcl
- post-run epcl
- in-run epcl
- test epcl or play back file
- channel file
- Thevenin dynamic model file
- generator dynamic model file

An example is shown below. Each run includes prerun_setGThevn.p as a pre-run epcl. The following Prerun_setGThevn.p are included in the test package and can be easily modified to any other desired short circuit ratio.

Table 5: Pre-run epcl to Set Short Circuit Ratio (SCR)

SCR	EPCL
1	prerun_setGThev1.p
2	prerun_setGThev2.p
2.5	prerun_setGThev2+.p
3	prerun_setGThev3.p
4	prerun_setGThev4.p
5	prerun_setGThev5.p
10	prerun_setGThev10.p
1000	prerun_setGThev0.p

flat run and summarize control settings

TestIBR.sav prerun_flat.p CheckREModels.p none Flat.p TestIBR_flat_3.chf Thevenin.dyd
TestIBR.dyd

bump test at SCR=3

TestIBR.sav prerun_setGThev3.p none none Bump.p TestIBR_bump_3.chf
Thevenin.dyd TestIBR.dyd

bump test at SCR=2

TestIBR.sav prerun_setGThev2.p none none Bump.p TestIBR_bump_2.chf
Thevenin.dyd TestIBR.dyd

PPC voltage reference step change test

TestIBR.sav prerun_setGThev3.p none none vstep_b.p TestIBR_vstep_3.chf
Thevenin.dyd TestIBR.dyd

PPC frequency reference step change test

TestIBR.sav prerun_setGThev3.p none none fstep_b.p TestIBR_fstep_3.chf
Thevenin.dyd TestIBR.dyd

vrt play-back

TestIBR.sav prerun_setGThev0.p none none play_vrt.csv TestIBR_vrt.chf
TheveninPB.dyd TestIBR.dyd

1.1.2 Model validation

Examine the dyd file visually. Verify proper and complete set of models are provided. Run IBR_model_test.p. Then review the simulation results.

Flat run and control setting review

Examine simulation log file and event file for the flat run and verify there are no errors and no events. The terminal voltage, active power and reactive power of the generators are all flat. The active power and reactive power have spread less than 1 MW/MVar or 1%. The voltage, active power and reactive power match the power flow condition.

Examine parametererrors.csv for suspicious parameters. It lists parameters that need verification.

Open controlmode.csv. Verify control mode and control gains against the control requirements.

Note the voltage regulation bus and monitored branch. The monitored branch should be in the direction of from the generator to the grid.

Bump test – large disturbance test

Bump.p applies a 3-phase-to-ground fault at the POI, then clears the fault after 4 cycles for interconnections above 200kV or 6 cycles for interconnections below 200kV. It is recommended to run bump tests at SCR = 3. Increase SCR if the bump test is unstable and report that the model is unstable at SCR = 3.

Examine simulation results of the bump run. **Plot *ipcmd* and *iqcmd*** from regc model. If one or both *ipcmd* and *iqcmd* go to 0, find out why. Check P/Q priority, control modes and current limits. The *iqcmd* should be in the right direction to control voltage. *iqcmd* should reach *iqmax* during the fault. Note overshoot of terminal voltage post-fault and how long it takes to settle. If there are multiple generating units modeled, plot all Qgens on the same plot and observe coordination among the units. Observe active power recovery after the fault. Note how long it takes for the active power to return to pre-fault level.

Voltage/reactive power reference step change test – small disturbance test

Depending on the control setup, either a voltage or reactive power reference step change test is performed. Select from the table below for the applicable test EPCL.

Table 6: Voltage/Reactive Power Reference Step Change Test EPCL

	Dynamic Model	Description	Notes
vstep_a.p	repc_a	Voltage or reactive power reference step change	The same code can be used for both voltage control (reflag=1) and reactive power control (reflag=0)
vstep_b.p	repc_b	Voltage reference step change	
qstep_b.p	repc_b	Reactive power reference step change	

The vstep test increases the PPC reference by 0.05 p.u. at t=5 sec, reduces PPC reference from the previous value by 0.1 p.u. at t=35 sec. Continue simulation for another 30 sec to give it enough time to settle. Depending on how fast the plant controls respond, the simulation time could be adjusted in the test EPCL.

The qstep_b test increases the PPC Q reference by 20 MVar at t=5 sec, reduces PPC reference from the previous value by 40 Mvar at t=35 sec. Continue simulation for another 30 sec to give it enough time to settle. The step change can be adjusted in the EPCL for the plant size being tested.

Examine simulation results. Plot *ipcmd* and *iqcmd* from regc model. *iqcmd* should ramp up in response to the increased reference. Observe whether the PPC controlled voltage or reactive power will reach the reference and how long it takes to reach the reference. *iqcmd* should ramp down in response to the reduced reference. Observe how well the voltage or reactive power is controlled.

Frequency reference step change test – small disturbance test

The test is only applicable if the plant has the primary frequency response enabled (frqflg=1). To verify the upward frequency response (baseload flag=0 and frqflg=1), active output in the power flow should be lower than Pmax. Select from the table below for the applicable test EPCL.

Table 7: Frequency Reference Step Change Test EPCL

	Dynamic Model	Description	Notes
fstep_a.p	repc_a	Frequency reference step change	
fstep_b.p	repc_b	Frequency reference step change	

The fstep test first reduces frequency reference by 0.3Hz at t=5 sec, then increase it by 0.6Hz at t=35 sec. Depending on how fast the plant controls respond, the simulation time could be adjusted in the test EPCL.

Examine simulation results. Plot ipcmd and iqcmd from regc model. iqcmd should ramp down first and up next in response to the reference changes. For 5% droop, the active power response would be about 9% of Pmax for 0.3Hz change with 0.036Hz control deadband. Observe how long it takes to reach the droop response.

Voltage ride through test

An infinite voltage source is used in the test such that the POI voltage is the same as the play-in voltage. Examine the simulation results to verify the generator rides through the entire simulation period.

Frequency ride through test

The test is not needed. Frequency ride-through settings can be reviewed with the PRC-024 spreadsheet tool.

1.2 WECC Full-Loop Test

There is no change to PTO's practice. The model is plugged into the WECC full-loop case. The bump test is performed and the performance is checked.