Inverter-Based Resources (IBR) Dynamic Model Validation Procedure

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Housekeeping reminders

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- Please keep comments professional and respectful.
- Please try and be brief and refrain from repeating what has already been said so that we can manage the time efficiently.

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  - Please remember to state your name and affiliation before making your comment.
- If you need technical assistance during the meeting, please send a chat to the event producer.
- You may also send your question via chat to either Kaitlin McGee or to all panelists.

Outline

- Existing required tests performed by Interconnection Customers (ICs)
- Proposed tests to be performed by ICs
- Demonstration of the test results on a sample case
- Processes require ICs providing the test results

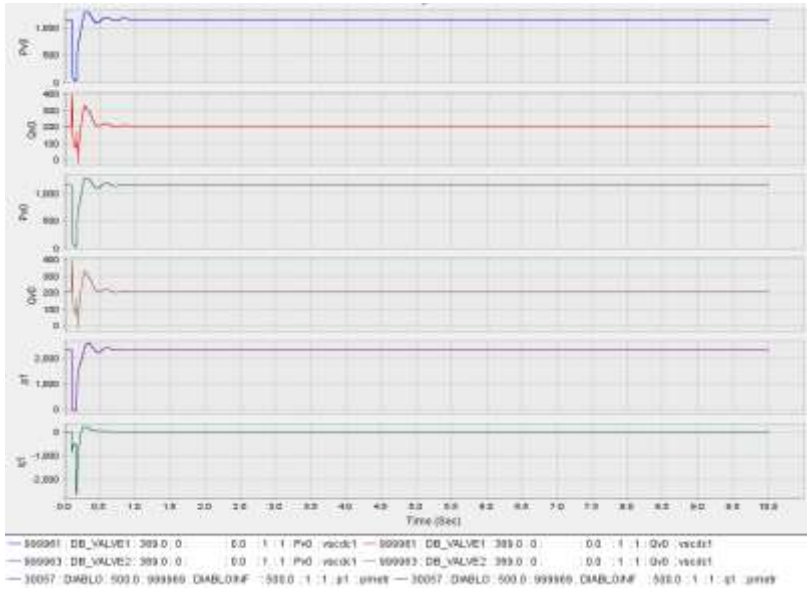
Existing tests performed by ICs

- Flat Run and Bump Test are currently performed by ICs as part of IR and MMA process.
- The objective of including these tests is to ensure the alignment between power flow model (.epc) and the dynamic model (.dyd) of the project.
- Flat run is a test in which no system disturbance is applied during the dynamic simulation and it is expected that system variables will remain constant for the duration of the dynamic simulation
- Bump Test is to apply a fault at POI and remove it after few cycles. It is expected that after a few seconds, all system parameters will return to pre-disturbance levels and remain constant
- the ICs are required to submit screenshots of plots for the results of these tests

Examples of Flat Run and Bump Test Results

Flat Run Test Result

Bump Test Result



Additional Tests Performed on IBR Models

- In addition to Flat Run and Bump Test performed by ICs as part of their application, the followings tests are currently performed on IBR models later on as part of IR review and MMA processes
  - Voltage (or Q) reference step change
  - Frequency reference step change
  - Voltage ride-through test
- To make the processes more efficient, the plan is to have ICs to perform the above tests as part of the IR and MMA processes and submit IBR dynamic models that pass all the tests

Detail Information on the Required Tests

- The “IBR Dynamic Model Validation Procedure.pdf” at the link below provides detailed description of the tests, how to perform them, and how to analyze the test results.

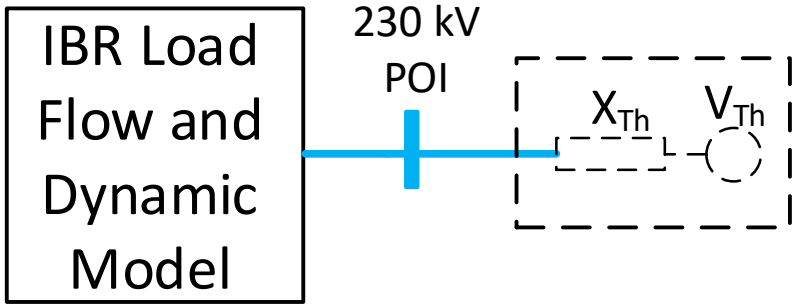
http://www.caiso.com/Documents/ISO-Inverter-Based-Model-Validation-Procedure.zip

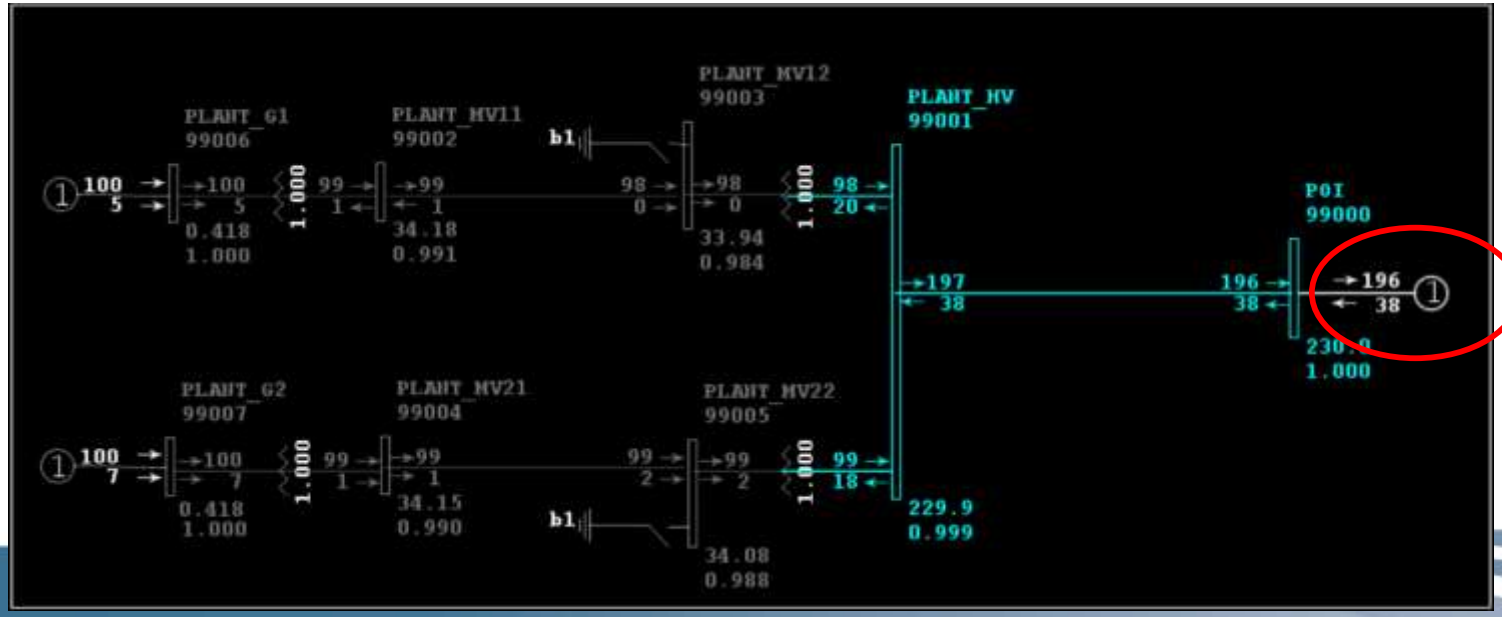
Folder	Description	Files
.	Working folder where PSLF is invoked	• IBR_model_test.p (main program) • prerun_setGThev*n*.p (set SCR to *n*) • CheckREModels.p (extract control settings) • Runs_IBR_Tests.runs (define test runs)
.\cases\	Power flow cases	*.sav
.\dyds\	Dynamic models and contingencies	• *.dyd (dynamic model) • Flat.p (flat run) • Bump.p (fault at POI) • Vstep_(a/b).p (plant controller voltage reference step change) • Fstep_(a/b).p (plant controller frequency reference step change) • Play_vrt.csv (play-back voltage signal for voltage fide-through test)
.\chans\	Simulation output files	*.log (simulation log file) *_event.csv (event file) *.chf (channel file)

- As detailed in the procedure, the tests will be performed on two system configurations: stand-alone and WECC full-loop

Stand-Alone Tests

- In the stand-alone test, the Flat Run and other tests are performed on an IBR model that is connected to a Thevenin equivalent of the system at POI.



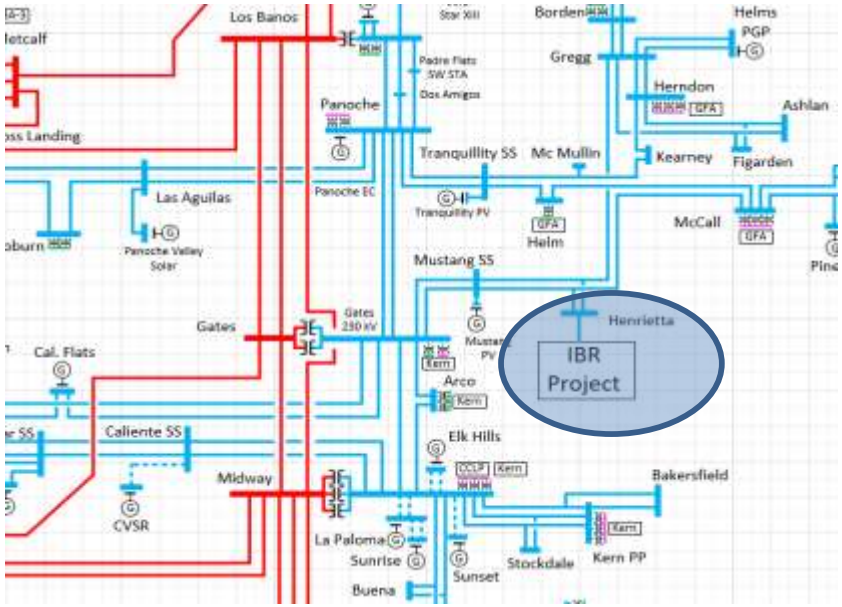


System is modeled as a voltage source behind an impedance (Thevenin Equivalent)

WECC Full-Loop Tests

- In WECC full-loop tests the dynamic performance of the IBR will be evaluated in the entire WECC system

- ICs are only required to provide the test results for stand-alone tests as part of IR and MMA processes
- The WECC full-loop tests are performed later in the process

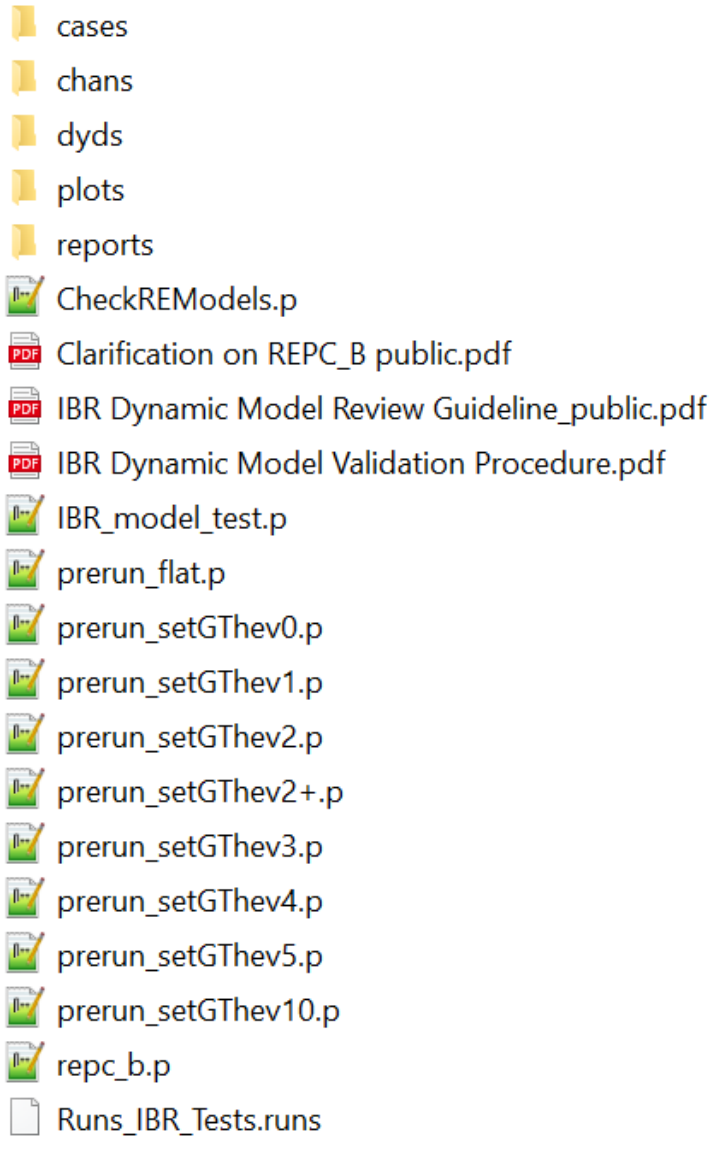


Stand-alone Test: Folder Setup

- http://www.caiso.com/Documents/ISO-Inverter-Based-Model-Validation-Procedure.zip zip file includes the listed folders and files

- EPCL codes have been developed to help performing the required tests.

- Setup the folder structure with the codes

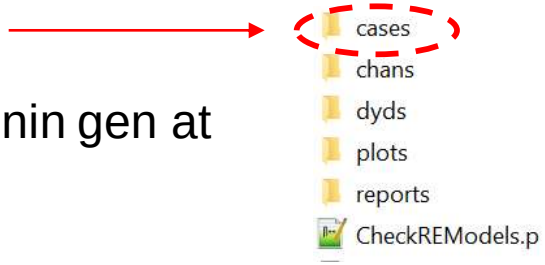


Stand-alone Test Process

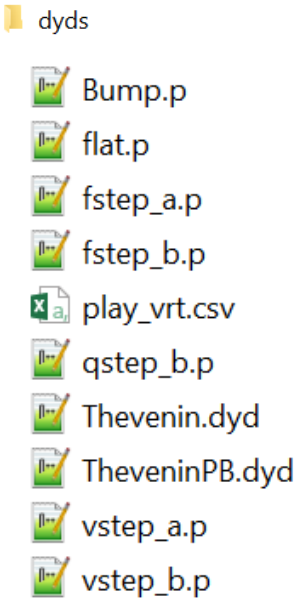
- Represent the grid at POI by a Thevenin generator
  - Thevenin generator MVA = plant MVA
  - Thevenin impedance is setup to represent the desired short circuit ratio (SCR) for model validation
- The tests will be performed at selected SCR
  - Flat run
  - Bump test
  - Voltage (or Q) reference step change
  - Frequency reference step change
  - Voltage ride-through test

Stand-alone Test: Input Data

- Power flow model folder (.\cases\)
  - POI bus type = 0 (swing bus); Thevenin gen at POI bus



- Dynamic model folder (.\dyds\)
  - Add IBR dynamic model submitted by IC
  - Modify the POI bus number in the following
    - Thevenin.dyd
    - TheveninPB.dyd
    - Bump.p
  - Modify the repc model ID in the following
    - Vstep_a.p and fstep_a.p if repc_a model
    - Vstep_b.p or fstep_b.p if repc_b model
  - Don’t change flat.p and Play_vrt.csv files



Test Run File

Specify the tests and SCR in the run file (Runs_IBR_tests.runs)

 # flat run and summarize control settings
TestIBR.sav prerun_setGThev3.p CheckREModels.p none Flat.p TestIBR_flat_3.chf Thevenin.dyd TestIBR.dyd

 # bump test at SCR=3
TestIBR.sav prerun_setGThev3.p none none Bump.p TestIBR_bump_3.chf Thevenin.dyd TestIBR.dyd

 # bump test at SCR=2
TestIBR.sav prerun_setGThev2.p none none Bump.p TestIBR_bump_2.chf Thevenin.dyd TestIBR.dyd

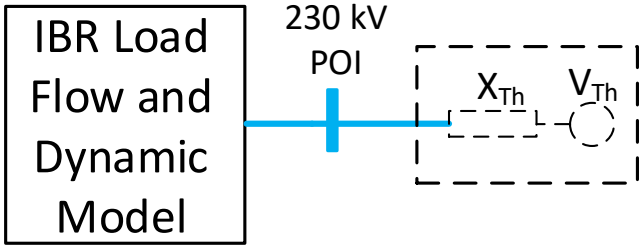
 # PPC voltage reference step change test
TestIBR.sav prerun_setGThev3.p none none vstep_b.p TestIBR_vstep_3.chf Thevenin.dyd TestIBR.dyd

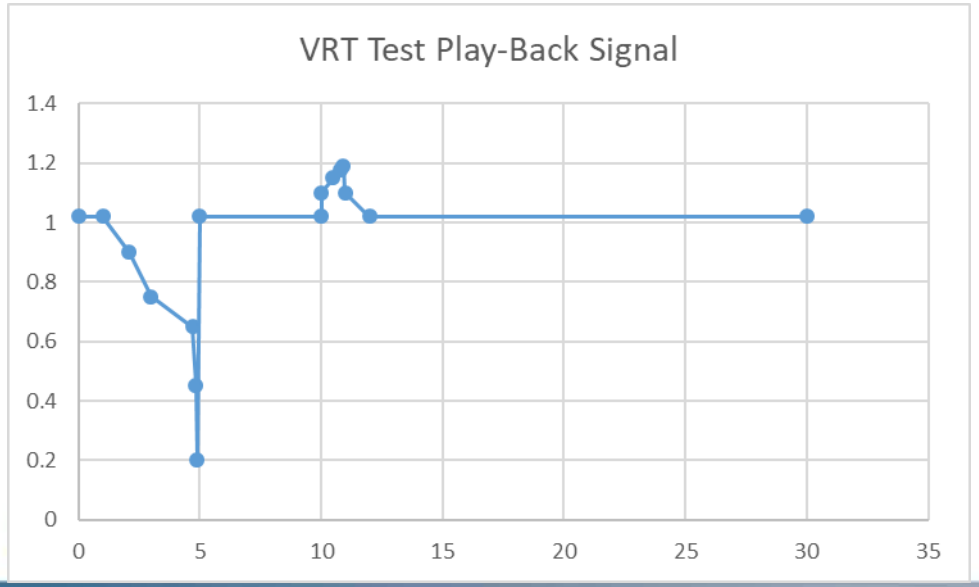
 # PPC frequency reference step change test
TestIBR.sav prerun_setGThev3.p none none fstep_b.p TestIBR_fstep_3.chf Thevenin.dyd TestIBR.dyd

 # vrt play-back
TestIBR.sav prerun_setGThev0.p none none play_vrt.csv TestIBR_vrt.chf TheveninPB.dyd TestIBR.dyd

Voltage Ride-Through Test

- The “prerun_setGThev0.p” code sets the Xth to a very low value and adjusts the source voltage over time based on the “play_vrt.csv” file shown in the plot.





Content of the play_vrt.csv” file

1.02 is the steady
0.0 1.02 60.0
1.0 1.02 60.0
2.1 0.9 60.0
3.0 0.75 60.0
4.7 0.65 60.0
4.85 0.45 60.0
4.9 0.2 60.0
5.0 1.02 60.0
10.0 1.02 60.0
10.02 1.1 60.0
10.5 1.15 60.0
10.8 1.175 60.0
10.9 1.19 60.0
11.0 1.1 60.0
12.0 1.02 60.0
30 1.02 60.0

PRC-024 Voltage Ride Through Requirement

Voltage (p.u.)	Duration (sec)
<=0.45	0.15
<=0.65	0.3
<=0.75	<2
<=0.9	<3
>=1.10	<1
>=1.15	<0.5
>=1.175	<0.2

Flat run and control setting review

- No errors and no events in the log file and event file
- V, P and Q are flat and match the power flow solution
  - If not flat, check whether it is flat at higher SCR
- Examine parametererrors.csv for suspicious parameters
- Review controlmode.csv and verify control mode and control gains against the control requirements.
- Note the voltage regulation bus and monitored branch in the dyd file. The monitored branch should be in the direction of from the generator to the grid.

Bump Test

- 3-phase-to-ground fault at POI
- Fault duration 4 to 6 cycles depending on the POI voltage
- Start with SCR = 3
- Examine simulation results
  - Plot ipcmd and iqcmd from regc model
  - Verify P/Q control priority; iqcmd in the right direction and magnitude
  - Observe post-fault overshoot and settling time
  - Verify proper coordination among generators if multiple-gen
- If unstable, increase SCR

Voltage Reference Step Change Test

- Depending on the repc control mode, the reference could be voltage or reactive power
- At t=5, increase the PPC voltage reference by 0.05 pu
- At t=35, reduce the PPC voltage reference by 0.1 pu
- Examine the simulation results
  - Plot ipcmd and iqcmd from regc model
  - Observe Qgen response and response time
  - Compare with the MOD-26 test

Frequency Reference Step Change Test

- The test is applicable if the plant has frequency response
- To test upward frequency response, pre-fault Pgen should be lower than Pmax
- At t=5, reduce the PPC freq reference by 0.3Hz
- At t=35, increase the PPC freq reference by 0.6Hz
- Examine the simulation results
  - Plot ipcmd and iqcmd from regc model
  - Observe Pgen response and response time
  - Compare with the MOD-27 test

Voltage Ride-Through Test

- Play the voltage signal at POI bus
- The IBR should ride-through the test
- Verify the IBR is not tripped and the Pgen/Qgen response is reasonable

IR and Modification process and IBR submittals

- Effective immediately, modifications and new interconnection request package submittals will require this IBR Model tool results to be submitted.

- It will be determined later the extent to which Cluster 15 applications will require the use of the IBR model tool.

Contact Information

- For modification-related questions, please contact your QM project manager or queuemanagement@caiso.com
- For queue cluster-related questions please contact irinfo@caiso.com

Next Steps: Comments

- Please submit comments on the discussion by end of day June 26, 2023 to initiativecomments@caiso.com.
- A comment template will be available on the Miscellaneous Meetings Page: http://www.caiso.com/informed/Pages/MeetingsEvents/MiscellaneousStakeholderMeetings/Default.aspx
- If you have any questions, please contact isostakeholderaffairs@caiso.com